SoC Security: Architecture, IP, or CAD?



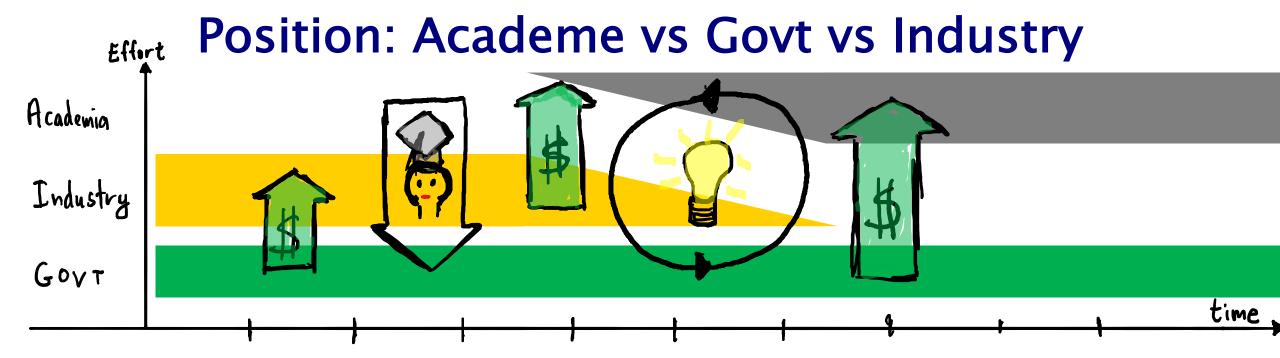
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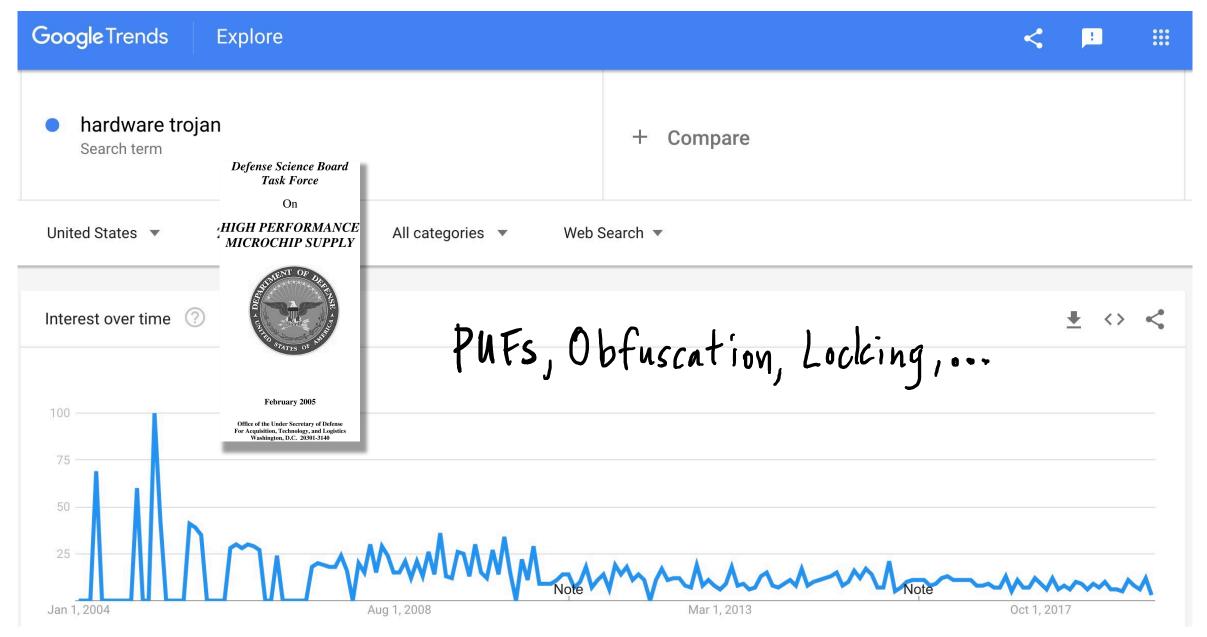
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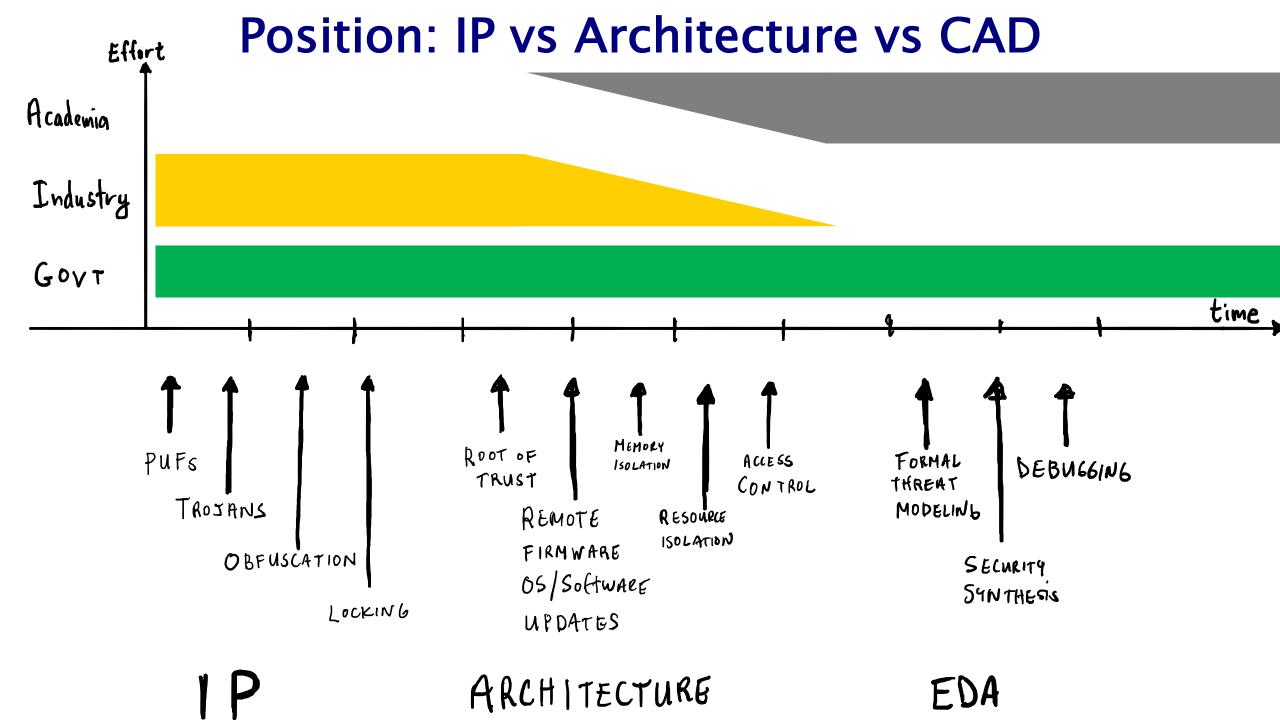
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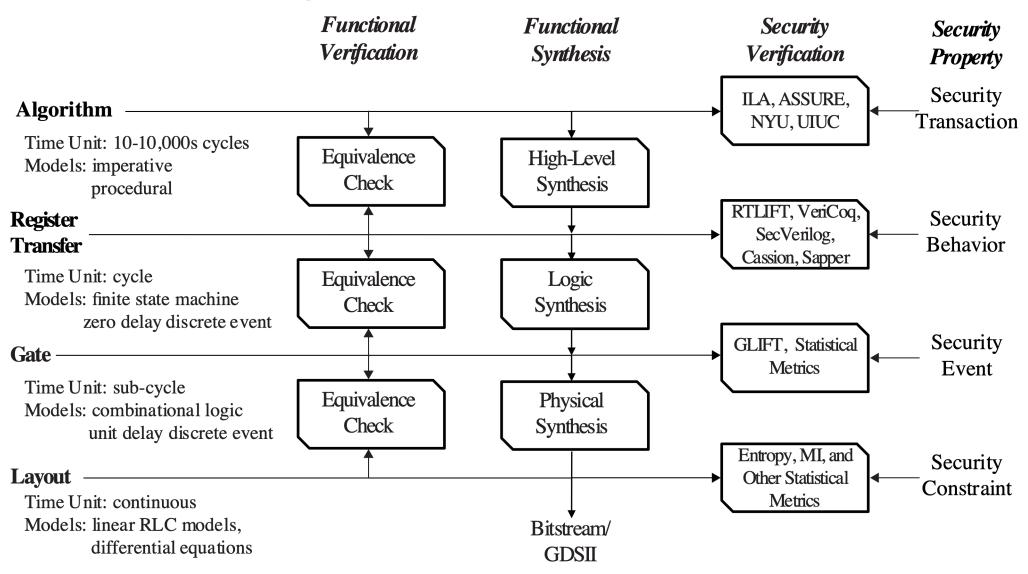


Position: IP Security is (mostly) solved





Pressing Need: Formal Threat Models



Wei Hu, Alric Althoff, Armaiti Ardeshiricham, and Ryan Kastner, "**Towards Property Driven Hardware Security**", *Microprocessor Test and Verification Conference*, December 2016 (pdf)

Pressing Needs/Challenges: Security Debugging

1) Write HW, SW, FW/, ...

```
input in:
output out:
output [7:0] counter;
req [7:0] counter:
wire counter_overflow = (counter == 8'hff);
wire counter_underflow = (counter == 8'h00);
always @(posedge clk or negedge xreset)
begin
        if (xreset == 0)
                counter <= 0:
        else if (en && in && !counter_overflow)
                counter <= counter + 1;
        else if (en && !in && !counter_underflow)
                counter <= counter - 1:
        else
                counter <= counter:
end
```

2) Write Security Properties 3)

```
assert isolation(request[0],request[1])
assert ...
```



4) Fix security flaws

- Security Experts 「_(ツ)

Issue!!

Hardware

Problem!

Security

- Hardware Designers _('

