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Education

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|---|------------------------|
| University of California, Los Angeles Doctor of Philosophy in Computer Science, September 2002 Thesis: Synthesis Techniques and Optimizations for Reconfigurable Systems Advisor: Professor Majid Sarrafzadeh | Los Angeles, CA |
| Northwestern University Master of Science Degree in Computer Engineering, August 2000 Thesis: Methods and Algorithms for Coupling Reduction Advisor: Professor Majid Sarrafzadeh | Evanston, IL |
| Northwestern University Bachelor of Science in Computer Engineering, June 1999 Bachelor of Science in Electrical Engineering, June 1999 | Evanston, IL |

Experience

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| UCSD Department of Computer Science and Engineering <i>Full Professor</i> – San Diego, CA | Sept 2007 - present |
| UCSB Department of Electrical and Computer Engineering <i>Assistant, Associate Professor</i> – Santa Barbara, CA | Sept 2002 – August 2007 |
| UCLA Computer Science Department <i>Graduate Research Assistant</i> – Los Angeles, CA | Sept 2000 – Sept 2002 |
| Northwestern University VLSI CAD Group <i>Graduate Research Assistant</i> – Evanston, IL | Jan 1999 – Aug 2000 |
| Computational Geometry and Algorithm Visualization Laboratory <i>Undergraduate Research Assistant</i> – Evanston, IL | Jun 1997 – Sept 1997 |

Honors

- Honorable Mention for IEEE Micro Top Pick: Xun Li, Vineeth Kashyap, Jason Oberg, Mohit Tiwari, Vasanth Rajarathinam, Ryan Kastner, Timothy Sherwood, Ben Hardekopf, and Frederic Chong, “Sapper: A Language for Hardware-Level Security Policy Enforcement”, Named as Honorable Mention in IEEE Micro's Top Picks from Computer Architecture Conferences, January-February 2015.
 - Best Paper Award: International Conference on Field Programmable Logic and Applications (FPL) Michael Servit Best Paper Award, 2014
 - IEEE Micro Top Pick: Hassan Wassel, Ying Gao, Jason Oberg, Ted Huffmire, Ryan Kastner, Frederic Chong, and Timothy Sherwood. “Networks-On-Chip with Provable Security Properties”, IEEE Micro: Micro's Top Picks from Computer Architecture Conferences, January-February 2014.
 - Community Award: International Conference on Field Programmable Logic and Applications (FPL) Community Award, 2013
 - UCSD Gordon Professional Fellow, 2011
 - N. N. Biswas Best Paper Award - Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Energy Efficient Hardware Synthesis of Polynomial Expressions”, *IEEE/ACM International Conference on VLSI Design*, January 2005
 - Best Teaching Assistant Award, 2001-2002 – UCLA Computer Science Department
 - Walter P. Murphy Fellowship, Northwestern University (1999 – 2000)
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Publications

Citations

- [Google Scholar](#)

- [Microsoft Academic Search](#)

Books

[B3] Ted Huffmire, Cynthia Irvine, Thuy Nguyen, Timothy Levin, Ryan Kastner and Timothy Sherwood, “Handbook on FPGA Design Security“, *Springer*, June 2010, ISBN-13: 9789048191567 ([order](#))

[B2] Ryan Kastner, Farzan Fallah, and Anup Hosangadi, “Arithmetic Optimization Techniques for Hardware and Software Design“, *Cambridge University Press*, May 2010, ISBN-13: 9780521880992 ([order](#))

[B1] Ryan Kastner, Adam Kaplan and Majid Sarrafzadeh, “Synthesis Techniques and Optimizations for Reconfigurable Systems“, *Kluwer Academic Publishers*, November 2003, ISBN 1402075983 ([order](#))

Book Chapters

[BC5] Bridget Benson and Ryan Kastner, “Design of a Low-Cost Underwater Acoustic Modem“, *Optical, Acoustic, Magnetic, and Mechanical Sensor Technologies*, Krzysztof Iniewski (editor), CRC Press, 2012

[BC4] Jonathan Valamehr, Ted Huffmire, Cynthia Irvine, Ryan Kastner, Cetin Kaya Koc, Timothy Levin and Timothy Sherwood, “A Qualitative Security Analysis of a New Class of 3-D Integrated Crypto Co-processors“, *Cryptography and Security: From Theory to Applications*, D. Naccache (editor), Springer, 2011 ([pdf](#))

[BC3] Gang Wang, Wenrui Gong and Ryan Kastner, “Operation Scheduling: Algorithms and Design Space Exploration“, *High Level Synthesis: From Algorithm to Digital Circuit*, Philippe Coussy and Adam Morawiec (editors), Springer Publishing Company, Netherlands, 2008 ([pdf](#))

[BC2] Elaheh Bozorgzadeh, Adam Kaplan, Ryan Kastner, Seda Ogrenci Memik, and Majid Sarrafzadeh, “Optimization for Reconfigurable Systems Using Hierarchical Abstraction“, *Multi-level Optimization and VLSI CAD*, J. Cong and J. R. Shinnerl (editors), Kluwer Academic Publishers, Boston, 2002 ([pdf](#))

[BC1] Elaheh Bozorgzadeh, Ryan Kastner, Seda Ogrenci Memik, and Majid Sarrafzadeh, “Strategically Programmable Systems“, *The Computer Engineering Handbook*, CRC Press, December 2001

Journal Articles

[J44] Matthew Jacobsen, Dustin Richmond, Matthew Hogains, and Ryan Kastner, “RIFFA 2.1: A Reusable Integration Framework for FPGA Accelerators“, *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, in press

[J43] Christopher Barngrover, Alric Althoff, Paul DeGuzman, and Ryan Kastner, “A Brain-Computer Interface (BCI) for the Detection of Mine-Like Objects in Side Scan Sonar Imagery“, *IEEE Journal of Oceanic Engineering*, in press

[J42] Diba Mirza, Perry Naughton, Curt Schurgers, and Ryan Kastner, “Real-time collaborative tracking for underwater networked systems“, *Ad Hoc Networks*, 2014 ([pdf](#))

[J41] Jinwang Yi, Diba Mirza, Ryan Kastner, Curt Schurgers, Paul Roberts, and Jules Jaffe, “ToA-TS: Time of arrival based joint time synchronization and tracking for mobile underwater systems“, *Ad Hoc Networks*, 2014 ([pdf](#))

[J40] Wei Hu, Dejun Mu, Jason Oberg, Baolei Mao, Mohit Tiwari, Timothy Sherwood, and Ryan Kastner, “Gate Level Information Flow Tracking for Security Lattices“, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Volume 20, Issue 1, November 2014 ([pdf](#))

[J39] Jason Oberg, Sarah Meiklejohn, Timothy Sherwood, and Ryan Kastner, “Leveraging Gate-Level Properties to Identify Hardware Timing Channels“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume 33, Issue 9, September 2014 ([pdf](#))

- [J38] Hassan Wassel, Ying Gao, Jason Oberg, Ted Huffmire, Ryan Kastner, Frederic Chong, and Timothy Sherwood, “Networks on Chip with Provable Security Properties“, *IEEE Micro*, Volume 34, Issue 3, May-June 2014 ([pdf](#))
- [J37] Christopher Barngrover, Ryan Kastner, and Serge Belongie, “Semi-Synthetic Versus Real World Sonar Training Data for the Classification of Mine-Like Objects“, *IEEE Journal of Oceanic Engineering*, January 2014 ([pdf](#))
- [J36] Feiyun Wu, Yuehai Zhou, Feng Tong, and Ryan Kastner, “Simplified p-norm-like Constraint LMS Algorithm for Efficient Estimation of Underwater Acoustic Channels“, *Journal of Marine Science and Application*, Volume 12, Issue 2, Pages 228-234 June 2013 ([pdf](#))
- [J35] Wei Hu, Jason Oberg, Janet Barrientos, Dejun Mu, and Ryan Kastner, “Expanding Gate Level Information Flow Tracking for Multi-level Security“, *IEEE Embedded Systems Letters*, Volume 5, Issue 2, June 2013 ([pdf](#))
- [J34] Tan Nguyen, Daniel Hefenbrock, Jason Oberg, Ryan Kastner, and Scott Baden, “A Software-Based Dynamic-Warp Scheduling Approach for Load-Balancing the Viola-Jones Face Detection Algorithm on GPUs“, *Journal of Parallel and Distributed Computing*, Volume 73, Issue 5, Pages 677–685, May 2013 ([pdf](#))
- [J33] Jonathan Valamehr, Timothy Sherwood, Ryan Kastner, David Marangoni-Simonsen, Ted Huffmire, Cynthia Irvine, and Timothy Levin, “A 3D Split Manufacturing Approach to Trustworthy System Development“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Special Section on Three-dimensional Integrated Circuits and Microarchitectures, Volume 32, Number 4, Pages 611-615, April 2013 ([pdf](#))
- [J32] Jason Oberg, Timothy Sherwood, and Ryan Kastner, “Eliminating Timing Information Flows in a Mix-trusted System-on-Chip“, *IEEE Design and Test of Computers*, March/April 2013 ([pdf](#))
- [J31] Wei Hu, Jason Oberg, Ali Irturk, Mohit Tiwari, Timothy Sherwood, Dejun Mu, and Ryan Kastner, “On the Complexity of Generating Gate Level Information Flow Tracking Logic“, *IEEE Transactions on Information Forensics and Security*, vol. 7, no. 3, June 2012 ([pdf](#))
- [J30] Lingjuan Wu, Jennifer Trezzo, Diba Mirza, Paul Roberts, Jules Jaffe, Yangyuan Wang and Ryan Kastner, “Designing an Adaptive Acoustic Modem for Underwater Sensor Networks“, *IEEE Embedded Systems Letters*, vol. 3, issue 3, December 2011 ([pdf](#))
- [J29] Henry Tat Kwong Tse, Pingfan Meng, Daniel R. Gossett, Ali Irturk, Ryan Kastner and Dino Di Carlo, “Strategies for Implementing Hardware-Assisted High-Throughput Cellular Image Analysis“, *Journal of Laboratory Automation*, vol. 16, no. 5, October 2011 ([pdf](#))
- [J28] Wei Hu, Jason Oberg, Ali Irturk, Mohit Tiwari, Timothy Sherwood, Dejun Mu and Ryan Kastner, “Theoretical Fundamentals of Gate Level Information Flow Tracking“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, issue 8, August 2011 ([pdf](#))
- [J27] Ali Irturk, Janarbek Matai, Jason Oberg, Jeffrey Su and Ryan Kastner, “Simulate and Eliminate: A Top-to-Bottom Design Methodology for Automatic Generation of Application Specific Architectures“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, issue 8, August 2011 ([pdf](#))
- [J26] Bridget Benson, Arash Arfaee, Choon Kim, Ryan Kastner and Rajesh Gupta, “Integrating Embedded Computing Systems into High School and Early Undergraduate Education“, *IEEE Transactions on Education*, vol. 54, issue 2, May 2011 ([pdf](#))
- [J25] Bridget Benson, Ying Li, Brian Faunce, Kenneth Domond, Don Kimball, Curt Schurgers and Ryan Kastner, “Design of a Low-Cost Underwater Acoustic Modem“, *IEEE Embedded Systems Letters*, vol. 2, issue 3, September 2010 ([pdf](#))
- [J24] Ted Huffmire, Brett Brotherton, Gang Wang, Timothy Sherwood, Ryan Kastner, Timothy Levin, Thuy D. Nguyen and Cynthia Irvine, “Security Primitives for Reconfigurable Hardware Based Systems“, *ACM Transactions on Reconfigurable Technology and Systems*, Vol. 3, Issue 2, May 2010 ([pdf](#))

- [J23] Ali Irturk, Bridget Benson, Shahnam Mirzaei and Ryan Kastner, “GUSTO: An Automatic Generation and Optimization Tool for Matrix Inversion Architectures“, *ACM Transactions on Embedded Computing Systems*, Vol. 9, No. 4, March 2010 ([pdf](#))
- [J22] Shahnam Mirzaei, Anup Hosangadi and Ryan Kastner, “Layout Aware Optimization of High Speed Fixed Coefficient FIR Filters for FPGAs“, *International Journal of Reconfigurable Computing*, Volume 2010, Article ID 697625, January 2010 ([pdf](#))
- [J21] Ted Huffmire, Brett Brotherton, Timothy Sherwood, Ryan Kastner, Timothy Levin, Thuy D. Nguyen and Cynthia Irvine, “Managing Security in FPGA-Based Embedded Systems“, *IEEE Design and Test of Computers*, November/December 2008 ([pdf](#))
- [J20] Ted Huffmire, Timothy Sherwood, Ryan Kastner and Tim Levin, “Enforcing Memory Policy Specifications in Reconfigurable Hardware“, *Computers and Security*, Vol. 27, No. 5-6, October 2008 ([pdf](#))
- [J19] Ted Huffmire, Brett Brotherton, Nicholas Callegari, Jonathan Valamehr, Jeff White, Ryan Kastner, and Tim Sherwood, “Designing Secure Systems on Reconfigurable Hardware“, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 13, Issue 3, article no. 44, July 2008 ([pdf](#))
- [J18] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Algebraic Methods for Optimizing Constant Multiplications in Linear Systems“, *Springer Journal of VLSI Signal Processing*, Vol. 49, Issue 1, pp. 31-50, October 2007 ([pdf](#))
- [J17] Gang Wang, Wenrui Gong, Brian DeRenzi and Ryan Kastner, “Exploring Time/Resource Tradeoffs by Solving Dual Scheduling Problems with the Ant Colony Optimization” *ACM Transactions on Design Automation of Electronic Systems*, Vol. 12, Issue 4, article no. 46, September 2007 ([pdf](#))
- [J16] Gang Wang, Wenrui Gong, Brian DeRenzi and Ryan Kastner, “Ant Colony Optimizations for Resource and Timing-Constrained Operation Scheduling “*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 26, June 2007, pp. 1010-29 ([pdf](#))
- [J15] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Optimizing Polynomial Expressions by Algebraic Factorization and Common Subexpression Elimination“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, Oct. 2006, pp. 2012-22 ([pdf](#))
- [J14] Gang Wang, Satish Sivaswamy, Cristinel Ababei, Kia Bazargan, Ryan Kastner and Elaheh Bozorgzadeh, “Statistical Analysis and Design of Hardwired Routing Pattern FPGAs“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 10, Oct. 2006, pp. 2088-102 ([pdf](#))
- [J13] Gang Wang, Wenrui Gong and Ryan Kastner, “Application Partitioning on Programmable Platforms Using the Ant Colony Optimization“, *Journal of Embedded Computing*, Vol. 2, Issue 1, 2006 ([pdf](#))
- [J12] Yan Meng, Wenrui Gong, Ryan Kastner and Timothy Sherwood, “Algorithm/Architecture Co-exploration for Designing Energy Efficient Channel Estimator” “*American Scientific Publishers Journal of Low Power Electronics*, December 2005 ([pdf](#))
- [J11] Yan Meng, Timothy Sherwood and Ryan Kastner, “Exploring the Limits of Leakage Power Reduction in Caches“, *ACM Transactions on Architecture and Code Optimization*, November 2005 ([pdf](#))
- [J10] Seda Ogrenci Memik, Ryan Kastner, Elaheh Bozorgzadeh, and Majid Sarrafzadeh, “A Scheduling Algorithm for Optimization and Planning in High-level Synthesis“, *ACM Transactions on Design Automation of Electronic Systems*, Vol. 10, No. 1, January 2005 ([pdf](#))
- [J9] Ankur Srivastava, Ryan Kastner, Chunhong Chen and Majid Sarrafzadeh, “Timing Driven Gate Duplication“, *IEEE Transactions on Very Large Scale Integrated Systems*, January 2004 ([pdf](#))
- [J8] Xiaojian Yang, Maogang Wang, Ryan Kastner, Soheil Ghiasi and Majid Sarrafzadeh, “Congestion Reduction during Placement with Provably Good Approximation Bound“, *ACM Transactions on Design Automation of Electronic Systems*, July 2003 ([pdf](#))
- [J7] Elaheh Bozorgzadeh, Ryan Kastner and Majid Sarrafzadeh, “Creating and Exploiting Flexibility in Steiner Trees“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, May 2003 ([pdf](#))

[J6] Ryan Kastner, Adam Kaplan, Seda Ogresci Memik, Elaheh Bozorgzadeh, “Instruction Generation for Hybrid Reconfigurable Systems“, *ACM Transactions on Design Automation of Electronic Systems*, October 2002 ([pdf](#))

[J5] Ryan Kastner, Elaheh Bozorgzadeh and Majid Sarrafzadeh, “Pattern Routing: Use and Theory for Increasing Predictability and Avoiding Coupling“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, July 2002 ([pdf](#))

[J4] Xiaojian Yang, Ryan Kastner and Majid Sarrafzadeh, “Congestion Estimation During Top-down Placement“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 2002 ([pdf](#))

[J3] Ankur Srivastava, Ryan Kastner and Majid Sarrafzadeh, “On the Complexity of Gate Duplication“, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, September 2001 ([pdf](#))

[J2] Kiarash Bazargan, Ryan Kastner and Majid Sarrafzadeh, “3-D Floorplanning: Simulated Annealing and Greedy Placement Methods for Reconfigurable Computing Systems“, *Design Automation for Embedded Systems – RSP’99 Special Issue*, August 2000 ([pdf](#))

[J1] Kiarash Bazargan, Ryan Kastner and Majid Sarrafzadeh, “Fast Template Placement for Reconfigurable Computing Systems“, *IEEE Design and Test – Special Issue on Reconfigurable Computing*, January – March 2000 ([pdf](#))

Refereed Conference Articles

[C120] Quentin Gautier, Alexandria Shearer, Janarbek Matai, Dustin Richmond, Pingfan Meng, and Ryan Kastner, “Real-time 3D Reconstruction for FPGAs: A Case Study for Evaluating the Performance, Area, and Programmability Trade-offs of the Altera OpenCL“, *International Conference on Field-Programmable Technology (FPT)*, December 2014 ([pdf](#))

[C119] Dajung Lee, Janarbek Matai, Brad Weals, and Ryan Kastner, “High Throughput Channel Tracking for JTRS Wireless Channel Emulation“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2014 – Short Paper Acceptance Rate 126/259 = 48.6% ([pdf](#))

[C118] Matthew Jacobsen, Siddarth Sampangi, Yoav Freund, and Ryan Kastner, “Improving FPGA Accelerated Tracking with Multiple Online Trained Classifiers“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2014 – Full Paper Acceptance Rate 62/259 = 23.9% ([pdf](#)) – Best Paper Award Nomination

[C117] Pingfan Meng, Matthew Jacobsen, Motoki Kimura, Vladimir Dergachev, Thomas Anantharaman, Michael Requa, and Ryan Kastner, “Hardware Accelerated Novel Optical De Novo Assembly for Large-Scale Genomes“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2014 – Full Paper Acceptance Rate 62/259 = 23.9% ([pdf](#)) – Michael Servit Best Paper Award

[C116] Janarbek Matai, Joo-Young Kim, and Ryan Kastner, “Energy Efficient Canonical Huffman Encoding“, *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, June 2014 – Full Paper Acceptance Rate 22/85 = 25.9% ([pdf](#))

[C115] Matthew Jacobsen, Pingfan Meng, Siddarth Sampangi, Ryan Kastner, “FPGA Accelerated Online Boosting for Multi-Target Tracking“, *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2014 – Short Paper Acceptance Rate 37/134 = 27.6% ([pdf](#))

[C114] Xun Li, Vineeth Kashyap, Jason Oberg, Mohit Tiwari, Vasanth Rajarathinam, Ryan Kastner, Timothy Sherwood, Ben Hardekopf, and Frederic T. Chong, “Sapper: A Language for Hardware-Level Security Policy Enforcement“, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2014 – Acceptance Rate 49/217 = 22.6% ([pdf](#))

[C113] Jingwang Yi, Diba Mirza, Curt Schurgers, and Ryan Kastner, “Joint Time Synchronization and Tracking for Mobile Underwater Systems“, *ACM International Conference on UnderWater Networks and Systems (WUWNet)*, November 2013 – Full Paper Acceptance Rate 11/55 = 20% ([pdf](#))

[C112] Motoki Kimura, Janabek Matai, Matthew Jacobsen, and Ryan Kastner, “A Low-Power AdaBoost-Based Object Detection Processor Using Haar-Like Features“, *IEEE International Conference on Consumer Electronics (ICCE-Berlin)*, September 2013 ([pdf](#))

[C111] Matthew Jacobsen and Ryan Kastner, “RIFFA 2.0: A Reusable Integration Framework for FPGA Accelerators“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2013 – Acceptance Rate 53/233 = 22.7% ([pdf](#))

[C110] Dustin Richmond, John McGarry, Ali Irturk, and Ryan Kastner, “A FPGA Design for High Speed Feature Extraction from a Compressed Measurement Stream“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2013 – Acceptance Rate 53/233 = 22.7% ([pdf](#))

[C109] Dajung Lee, Pingfan Meng, Matthew Jacobsen, Henry Tse, Dino Di Carlo, and Ryan Kastner, “A Hardware Accelerated Approach for Imaging Flow Cytometry“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2013 – Acceptance Rate 53/233 = 22.7% ([pdf](#))

[C108] Xun Li, Vineeth Kashyap, Jason Oberg, Mohit Tiwari, Vasanth Rajarathinam, Ryan Kastner, Timothy Sherwood, Ben Hardekopf, and Frederic T. Chong, “Sapper: A Language for Provable Hardware Policy Enforcement“, *Workshop on Programming Languages and Analysis for Security (PLAS)*, June 2013 ([pdf](#))

[C107] Hassan M. G. Wassel, Ying Gao, Jason K. Oberg, Ted Huffmire, Ryan Kastner, Frederic T. Chong, and Timothy Sherwood, “SurfNoC: A Low Latency and Provably Non-Interfering approach to Secure Networks-On-Chip“, *International Symposium on Computer Architecture (ISCA)*, June 2013 – Acceptance Rate = 19% ([pdf](#))

[C106] Diba Mirza, Paul Roberts, Jinwang Yi, Curt Schurgers, Ryan Kastner and Jules Jaffe, “Energy Efficient Signaling Strategies for Tracking Mobile Underwater Vehicles“, *IEEE International Symposium on Underwater Technology (UT)*, March 2013 ([pdf](#))

[C105] Jason Oberg, Sarah Meiklejohn, Timothy Sherwood and Ryan Kastner, “A Practical Testing Framework for Isolating Hardware Timing Channels“, *Design Automation and Test in Europe (DATE)*, March 2013 – Interactive Presentation Acceptance Rate 302/829 = 36.4% ([pdf](#))

[C104] Pingfan Meng, Matthew Jacobsen and Ryan Kastner, “FPGA-GPU-CPU Heterogenous Architecture for Real-time Cardiac Physiological Optical Mapping“, *International Conference on Field-Programmable Technology (FPT)*, December 2012 – Short Paper Acceptance Rate: 52/114 = 45.6% ([pdf](#))

[C103] Janabek Matai, Pingfan Meng, Lingjuan Wu, Brad Weals and Ryan Kastner, “Designing a Hardware in the Loop Wireless Digital Channel Emulator for Software Defined Radio“, *International Conference on Field-Programmable Technology (FPT)*, December 2012 – Acceptance Rate: 24/114 = 21% ([pdf](#))

[C102] Diba Mirza, Curt Schurgers and Ryan Kastner, “Real-time Collaborative Tracking for Underwater Networked Systems“, *International Conference on Underwater Networks and Systems (WUWNet)*, November 2012 ([pdf](#))

[C101] Wei Hu, Jason Oberg, Dejun Mu and Ryan Kastner, “Simultaneous Information Flow Security and Circuit Redundancy in Boolean Gates“, *International Conference on Computer-Aided Design (ICCAD)*, November 2012 – Acceptance Rate 82/338 = 24.3% ([pdf](#))

[C100] Pingfan Meng, Ali Irturk, Ryan Kastner, Andrew McCulloch, Jeffrey Omens and Adam Wright, “GPU Acceleration of Optical Mapping Algorithm for Cardiac Electrophysiology“, *International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, August 2012 ([pdf](#))

[C99] Ryan Kastner, Albert Lin, Curt Schurgers, Jules Jaffe, Peter Franks and Brent S. Stewart, “Sensor Platforms for Multimodal Underwater Monitoring“, *International Green Computing Conference (IGCC)*, June 2012 – Invited Paper ([pdf](#))

[C98] Matthew Jacobsen, Yoav Freund and Ryan Kastner, “RIFFA: A Reusable Integration Framework for FPGA Accelerators“, *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 2012 – Short Paper Acceptance Rate 38/121 = 31.4%, ([pdf](#))

- [C97] Christopher Barngrover, Thomas Denewiler, Greg Mills and Ryan Kastner, “The Stingray AUV: A Small and Cost-Effective Solution for Ecological Monitoring“, *IEEE Oceans*, September 2011 ([pdf](#))
- [C96] Christopher Barngrover, Serge Belongie and Ryan Kastner, “JBoost Optimization of Object Detectors for Autonomous Underwater Vehicle Navigation“, *International Conference on Computer Analysis of Images and Patterns (CAIP)*, August 2011 – Acceptance Rate $138/286 = 48.3\%$ ([pdf](#))
- [C95] Ted Huffmire, Timothy Levin, Cynthia Irvine, Ryan Kastner and Timothy Sherwood, “3-D Extensions for Trustworthy Systems“, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2011 – Invited Paper ([pdf](#))
- [C94] Ryan Kastner, Jason Oberg, Wei Hu, and Ali Irturk, “Enforcing Information Flow Guarantees in Reconfigurable Systems with Mix-Trusted IP“, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2011 – Invited Paper ([pdf](#))
- [C93] Wei Hu, Jason Oberg, Ali Irturk, Mohit Tiwari, Timothy Sherwood, Dejun Mu, and Ryan Kastner, “An Improved Encoding Technique for Gate Level Information Flow Tracking“, *International Workshop on Logic and Synthesis (IWLS)*, June 2011 ([pdf](#))
- [C92] Mohit Tiwari, Jason Oberg, Xun Li, Jonathan K Valamehr, Timothy Levin, Ben Hardekopf, Ryan Kastner, Frederic T. Chong, and Timothy Sherwood, “Crafting a Usable Microkernel, Processor, and I/O System with Strict and Provable Information Flow Security“, *International Symposium of Computer Architecture (ISCA)*, June 2011 – Acceptance Rate: $40/208 = 19.2\%$ ([pdf](#))
- [C91] Jason Oberg, Wei Hu, Ali Irturk, Mohit Tiwari, Timothy Sherwood, and Ryan Kastner, “Information Flow Isolation in I2C and USB“, *Design Automation Conference (DAC)*, June 2011 – Acceptance Rate: $156/690 = 22.6\%$ ([pdf](#))
- [C90] Janarbek Matai, Ali Irturk and Ryan Kastner, “Design and Implementation of an FPGA-based Real-Time Face Recognition System“, *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2011 – Short Paper Acceptance Rate: $42/119 = 35.3\%$ ([pdf](#))
- [C89] Jonathan Valamehr, Mohit Tiwari, Timothy Sherwood, Ryan Kastner, Ted Huffmire, Cynthia Irvine and Timothy Levin, “Hardware Assistance for Trustworthy Systems through 3-D Integration“, *Annual Computer Security Applications Conference (ACSAC)*, December 2010 – Acceptance Rate: $39/227 = 17.2\%$ ([pdf](#))
- [C88] Ted Huffmire, Timothy Levin, Michael Bilzor, Cynthia Irvine, Jonathan Valamehr, Mohit Tiwari, Timothy Sherwood and Ryan Kastner, “Hardware Trust Implications of 3-D Integration“, *Workshop on Embedded Systems Security*, October 2010 ([pdf](#))
- [C87] Feng Tong, Shengyong Zhou, Bridget Benson and Ryan Kastner, “R&D of a Dual Mode Acoustic Modem Testbed for Shallow Water Channels“, *International Workshop on Underwater Networks (WUWNet)*, September 2010 ([pdf](#))
- [C86] Deborah Goshorn, Junguk Cho, Ryan Kastner and Shahnam Mirzaei, “Field Programmable Gate Array Implementation of Parts-based Object Detection for Real Time Video Applications“, *International Conference on Field Programmable Logic and Applications (FPL)*, September 2010 – Short Paper Acceptance Rate $103/226 = 45.6\%$ ([pdf](#))
- [C85] Jason Oberg, Wei Hu, Ali Irturk, Mohit Tiwari, Timothy Sherwood and Ryan Kastner, “Theoretical Analysis of Gate Level Information Flow Tracking“, *Design Automation Conference (DAC)*, June 2010 – Acceptance Rate: $148/607 = 24.4\%$ ([pdf](#))
- [C84] Ying Li, Xing Zhang, Bridget Benson and Ryan Kastner, “Hardware Implementation of Symbol Synchronization for Underwater FSK“, *IEEE International Conference on Sensor Networks, Ubiquitous, and Trustworthy Computing*, June 2010 ([pdf](#))
- [C83] Feng Tong, Bridget Benson, Ying Li and Ryan Kastner, “Channel equalization based on data reuse LMS algorithm for shallow water acoustic communication“, *IEEE International Conference on Sensor Networks, Ubiquitous, and Trustworthy Computing*, June 2010 ([pdf](#))

[C82] Bridget Benson, Ying Li, Ryan Kastner, Brian Faunce, Kenneth Domond, Donald Kimball and Curt Schurgers, “Design of a Low-Cost, Underwater Acoustic Modem for Short-Range Sensor Networks“, *IEEE Oceans*, May 2010 ([pdf](#))

[C81] Jung Uk Cho, Bridget Benson, Sunsern Cheamanukul and Ryan Kastner, “Increased Performace of FPGA-Based Color Classification System“, *IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2010 ([pdf](#))

[C80] Daniel Hefenbrock, Jason Oberg, Nhat Tan Nguyen Thanh, Ryan Kastner and Scott B. Baden, “Accelerating Viola-Jones Face Detection to FPGA-Level using GPUs“, *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2010 – Full Paper Acceptance Rate: $24/132 = 18.2\%$ ([pdf](#))

[C79] Jung Uk Cho, Bridget Benson and Ryan Kastner, “Hardware Acceleration of Multi-view Face Detection“, *IEEE Symposium on Application Specific Processors (SASP)*, July 2009 ([pdf](#))

[C78] Bridget Benson, Arash Arfaee, Choon Kim, Ryan Kastner and Rajesh Gupta, “Integrating Embedded Computing Systems into High School and Early Undergraduate Education“, *International Conference on Microelectronic Systems Education (MSE)*, July 2009 ([pdf](#))

[C77] Ying Li, Bridget Benson, Ryan Kastner and Xing Zhang, “Bit Error Rate, Power and Area Analysis of Multiple Implementations of Underwater FSK“, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2009 ([pdf](#))

[C76] Jung Uk Cho, Bridget Benson, Shahnam Mirzaei and Ryan Kastner, “Parallelized Architecture of Multiple Classifiers for Face Detection“, *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, July 2009 – Acceptance Rate: $25/70 = 35.7\%$ ([pdf](#))

[C75] Arash Arfaee, Ali Irturk, Farzan Fallah and Ryan Kastner, “Xquasher: A Tool for Efficient Computation of Multiple Linear Expressions“, *Design Automation Conference (DAC)*, July 2009 – Acceptance Rate: 21% ([pdf](#))

[C74] Bridget Benson, Ali Irturk, Junguk Cho and Ryan Kastner, “Energy Benefits of Reconfigurable Hardware for Use in Underwater Sensor Nets“, *IEEE Reconfigurable Architectures Workshop (RAW)*, May 2009 ([pdf](#), [slides](#))

[C73] Ali Irturk, Bridget Benson, Nikolay Laptev and Ryan Kastner, “Architectural Optimization of Decomposition Algorithms for Wireless Communication Systems“, *IEEE Wireless Communications and Networking Conference (WCNC)*, April 2009 – Acceptance Rate: $>500/1195 = \sim 46\%$ ([pdf](#), [slides](#))

[C72] Jung Uk Cho, Shahnam Mirzaei, Jason Oberg and Ryan Kastner “FPGA-Based Face Detection System Using Haar Classifiers“, *International Symposium on Field Programmable Gate Arrays (FPGA)*, February 2009 – Acceptance Rate: $24/92 = 26\%$ ([pdf](#))

[C71] Ali Irturk, Bridget Benson, Arash Arfaee and Ryan Kastner, “Automatic Generation of Decomposition based Matrix Inversion Architectures“, *IEEE International Conference on Field-Programmable Technology (FPT)*, December 2008 – Short Paper Acceptance Rate: $65/135 = 48.1\%$ ([pdf](#))

[C70] Ali Irturk, Bridget Benson, Nikolay Laptev and Ryan Kastner, “FPGA Acceleration of Mean Variance Framework for Optimal Asset Allocation“, *Workshop on High Performance Computational Finance*, November 2008 ([pdf](#))

[C69] Bridget Benson, Ali Irturk, Jung Uk Cho and Ryan Kastner, “Survey of Hardware Platforms for an Energy Efficient Implementation of Matching Pursuits Algorithm for Shallow Water Networks“, *International Workshop on Underwater Networks (WUWNet)*, September 2008 ([pdf](#))

[C68] Ryan Kastner and Ted Huffmire, “Threats and Challenges in Reconfigurable Hardware Security“, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2008 – Invited Paper ([pdf](#))

[C67] Shahnam Mirzaei, Ali Irturk, Ryan Kastner, Brad T. Weals and Richard E. Cagley “Design Space Exploration of a Cooperative MIMO Receiver for Reconfigurable Architectures“, *IEEE International*

Conference on Application-specific Systems, Architectures and Processors (ASAP), July 2008 – Acceptance Rate: 31% ([pdf](#))

[C66] Ali Irturk, Bridget Benson, Shahnam Mirzaei and Ryan Kastner, “An FPGA Design Space Exploration Tool for Matrix Inversion Architectures”□, *IEEE Symposium on Application Specific Processors (SASP)*, June 2008 ([pdf](#))

[C65] Ted Huffmire, Timothy Sherwood, Ryan Kastner, Timothy Levin, Thuy Nguyen and Cynthia Irvine, “Trustworthy System Security through 3-D Integrated Hardware”, *IEEE International Workshop on Hardware-Oriented Security and Trust (HOST)*, June 2008 ([pdf](#))

[C64] Bridget Benson, Frank Spada, Derek Manov, Grace Chang and Ryan Kastner, “Real Time Telemetry Options for Ocean Observing Systems”, *European Telemetry Conference*, April 2008 ([pdf](#), [slides](#))

[C63] Ryan Kastner, Wenrui Gong, and Gang Wang, “Ant Colony Optimization for High Level Synthesis”□, *Workshop on the High-Level Synthesis: “The New Wave of the High-Level Synthesis*, in conjunction with the *Design, Automation and Test in Europe Conference (DATE)*, March 2008

[C62] Frank Spada, Derek Manov, Grace Chang, Bridget Benson, and Ryan Kastner, “Real-time Telemetry Technologies for Moored Oceanographic Applications”, *Ocean Sciences Meeting*, March 2008 – poster presentation

[C61] Susmit Biswas, Gang Wang, Tzvetan S. Metodiev, Ryan Kastner, and Fredric T. Chong, “Combining Static and Dynamic Defect-Tolerance Techniques for Nanoscale Memory Systems”, *International Conference on Computer-Aided Design (ICCAD)*, November 2007 – Acceptance Rate: 26% ([pdf](#))

[C60] Susmit Biswas, Tzvetan Metodiev, Ryan Kastner and Fredric T. Chong, “A Pageable, Defect-Tolerant Nanoscale Memory Architecture”, *International Symposium on Nanoscale Architectures (NanoArch)*, October 2007 – Acceptance Rate: $139/510 = 27.3\%$ ([pdf](#), [slides](#))

[C59] Susmit Biswas, Tzvetan S. Metodiev, Fredric T. Chong, Ryan Kastner and Timothy Sherwood, “Efficient Storage of Defect Maps for Nanoscale Memory”□, *Workshop on Non-Silicon Computing* held in conjunction with the *International Symposium on Computer Architecture (ISCA)*, June 2007 ([pdf](#), [slides](#))

[C58] Ted Huffmire, Brett Brotherton, Gang Wang, Timothy Sherwood, Ryan Kastner, Timothy Levin, Thuy Nguyen and Cynthia Irvine, “Moats and Drawbridges: An Isolation Primitive for Reconfigurable Hardware Based Systems”, *IEEE Symposium on Security and Privacy*, May 2007 – Acceptance Rate: $29/246 = 11.8\%$ ([pdf](#), [slides](#))

[C57] Richard E. Cagley, Brad T. Weals, Scott A. McNally, Ronald Iltis, Shahnam Mirzaei and Ryan Kastner, “Implementation of the Alamouti OSTBC to a Distributed Set of Single-Antenna Wireless Nodes”□, *IEEE Wireless Communications and Networking Conference (WCNC)*, March 2007 – Acceptance Rate: $815/1721 = 47.4\%$ ([pdf](#), [slides](#))

[C56] Shahnam Mirzaei, Ryan Kastner, Richard E. Cagley and Bradley T. Weals “Memory Efficient Implementation of Correlation Function in Wireless Applications”, *International Symposium on Field Programmable Gate Arrays (FPGA)*, February 2007 – poster presentation

[C55] Ronald Iltis, Shahnam Mirzaei, Ryan Kastner, Richard E. Cagley and Brad T. Weals, “Carrier Offset and Channel Estimation for Cooperative MIMO Sensor Networks”, *IEEE Global Telecommunications Conference (GLOBECOM)*, November 2006 – Acceptance Rate: $1024/2548 = 40.2\%$ ([pdf](#), [slides](#))

[C54] Gang Wang, Wenrui Gong and Ryan Kastner, “On the Use of Bloom Filters for Defect Maps in Nanocomputing”□, *International Conference on Computer-Aided Design (ICCAD)*, November 2006 – Acceptance Rate: $135/537 = 25.1\%$ ([pdf](#))

[C53] Daniel Doonan, Tricia Fu, Christopher Utley, Ronald A. Iltis, Ryan Kastner and Hua Lee, “Design and Experimentation with a Software-Defined Acoustic Telemetry Modem”, *International Telemetering Conference (ITC)*, October 2006 ([pdf](#))

[C52] Shahnam Mirzaei, Anup Hosangadi and Ryan Kastner, “FPGA Implementation of High Speed FIR Filter Using Add and Shift Method”, *International Conference on Computer Design (ICCD)*, October 2006 – Acceptance Rate: 31% ([pdf](#), [slides](#))

[C51] Bridget Benson, Grace Chang, Derek Manov, Brian Graham and Ryan Kastner, “Design of a Low-cost Acoustic Modem for Moored Oceanographic Applications”, *International Workshop on Underwater Networks (WUWNet)*, September 2006 ([pdf](#), [slides](#))

[C50] Hua Lee, Tricia Fu, Daniel Doonan, Christopher Utley, Ronald A. Iltis and Ryan Kastner, “Design and Development of a Software-Defined Underwater Acoustic Modem for Sensor Networks for Environmental and Ecological Research”, *MTS/IEEE Oceans*, September 2006 ([pdf](#))

[C49] Theodore Huffmire, Shreyas Prasad, Timothy Sherwood and Ryan Kastner, “Policy-Driven Memory Protection for Reconfigurable Hardware”, *European Symposium on Research in Computer Security (ESORICS)*, September 2006 – Acceptance Rate: $32/160 = 20\%$ ([pdf](#))

[C48] Gang Wang, Wenrui Gong, Brian DeRenzi and Ryan Kastner, “Design Space Exploration using Time and Resource Duality with the Ant Colony Optimization”, *Design Automation Conference (DAC)*, July 2006 – Acceptance Rate: $209/865 = 24.2\%$ ([pdf](#), [slides](#))

[C47] Yan Meng, Timothy Sherwood and Ryan Kastner, “Leakage Power Reduction of Embedded Memories on FPGAs through Location Assignment”, *Design Automation Conference (DAC)*, July 2006 – Acceptance Rate: $209/865 = 24.2\%$ ([pdf](#), [slides](#))

[C46] Gang Wang, Wenrui Gong, and Ryan Kastner, “Defect-Tolerant Nanocomputing Using Bloom Filters”, *Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 2006 – poster presentation ([pdf](#))

[C45] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Optimizing High Speed Arithmetic Circuits Using Three Term Extraction”, *Design, Automation and Test in Europe Conference (DATE)*, March 2006 – Acceptance Rate: $267/834 = 32\%$ ([pdf](#), [slides](#))

[C44] Ryan Kastner, Wenrui Gong, Adam Kaplan, Philip Brisk, Majid Sarrafzadeh, Xin Hao, and Forrest Brewer, “Layout Driven Data Communication Optimization for High Level Synthesis”, *Design, Automation and Test in Europe Conference (DATE)*, March 2006 – Acceptance Rate: $267/834 = 32\%$ ([pdf](#), [slides](#))

[C43] Shahnam Mirzaei, Anup Hosangadi, and Ryan Kastner, “High Speed FIR Filter Implementation Using Add and Shift Method”, *International Symposium on Field Programmable Gate Arrays (FPGA)*, February 2006 – poster presentation

[C42] Yan Meng, Ryan Kastner and Timothy Sherwood, “Algorithm/Architecture Co-exploration for Designing Energy Efficient Wireless Channel Estimator”, *Mobile Computing Hardware Architectures: Design and Implementation (MOCHA)*, co-located with the *Hawaii International Conference on System Sciences (HICSS)*, January 2006 ([pdf](#))

[C41] Andrew P. Brown, Ronald A. Iltis and Ryan Kastner, “Efficient Distributed Algorithms for Data Fusion and Node Localization in Mobile Ad-hoc Networks”, *International Conference on Mobile Ad-hoc and Sensor Systems (MASS)*, November 2005 – Acceptance Rate: 33% ([pdf](#), [slides](#))

[C40] Wenrui Gong, Gang Wang and Ryan Kastner “Storage Assignment during High-level Synthesis for Configurable Architectures”, *International Conference on Computer-Aided Design (ICCAD)*, November 2005 – Acceptance Rate: 25% ([pdf](#), [slides](#))

[C39] Ronald A. Iltis, Hua Lee, Ryan Kastner, Daniel Doonan, Tricia Fu, Rachael Moore and Maurice Chin, “An Underwater Acoustic Telemetry Modem for Eco-Sensing”, *MTS/IEEE Oceans*, September 2005 ([pdf](#), [slides](#))

[C38] Wenrui Gong, Yan Meng, Gang Wang, Ryan Kastner and Timothy Sherwood, “Data Partitioning for Reconfigurable Architectures with Distributed Block RAM”, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, June 2005 ([pdf](#))

[C37] Yan Meng, Andrew P. Brown, Timothy Sherwood, Ronald A. Iltis, Hua Lee and Ryan Kastner, “MP Core: Algorithm and Design Techniques for Efficient Channel Estimation in Wireless Applications”, *Design Automation Conference (DAC)*, June 2005 – Acceptance Rate: 154/735 = 21.0% ([pdf](#), [slides](#))

[C36] Wenrui Gong, Gang Wang and Ryan Kastner, “Data Partitioning for Reconfigurable Architectures with Distributed Block RAM”, *International Workshop on Logic and Synthesis (IWLS)*, June 2005 ([pdf](#), [slides](#))

[C35] Ryan Kastner, Wenrui Gong, Xin Hao, Forrest Brewer, Adam Kaplan, Philip Brisk and Majid Sarrafzadeh, “Physically Aware Data Communication Optimization for Hardware Synthesis”, *International Workshop on Logic and Synthesis (IWLS)*, June 2005 ([pdf](#), [slides](#))

[C34] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Simultaneous Optimization of Delay and Number of Operations in Multiplierless Implementation of Linear Systems”, *International Workshop on Logic and Synthesis (IWLS)*, June 2005 ([pdf](#)) – poster presentation

[C33] Gang Wang, Wenrui Gong and Ryan Kastner, “Instruction Scheduling Using MAX-MIN Ant Colony Optimization”, *Great Lakes Symposium on Very Large Scale Integration (GLSVLSI)*, April 2005 – Full Paper Acceptance Rate: 52/239 = 21.8% ([pdf](#), [slides](#))

[C32] Satish Sivaswamy, Gang Wang, Cristinel Ababei, Kia Bazargan, Ryan Kastner and Elaheh Bozorgzadeh, “HARP: Hard-wired Routing Pattern FPGAS”, *International Symposium on Field Programmable Gate Arrays (FPGA)*, February 2005 – Acceptance Rate: 24/100 = 24% ([pdf](#), [slides](#))

[C31] Yan Meng, Timothy Sherwood and Ryan Kastner, “On the Limits of Leakage Power Reduction in Caches”, *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2005 – Acceptance Rate: 15.46% ([pdf](#), [slides](#))

[C30] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Reducing Hardware Complexity of Linear DSP Systems by Iteratively Eliminating Two Term Common Subexpressions”, *Asia South Pacific Design Automation Conference (ASP-DAC)*, January 2005 – Full Paper Acceptance Rate: 14.3% ([pdf](#), [slides](#))

[C29] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Energy Efficient Hardware Synthesis of Polynomial Expressions”, *International Conference on VLSI Design*, January 2005 – Acceptance Rate: 97/352 = 27.6% ([pdf](#), [slides](#)) - N. N. Biswas Best Student Paper Award

[C28] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Factoring and Eliminating Common Subexpressions in Polynomial Expressions”, *International Conference on Computer-Aided Design (ICCAD)*, November 2004 – Acceptance Rate: 24.42% ([pdf](#), [slides](#))

[C27] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Common Subexpression Elimination Involving Multiple Variables for Linear DSP Synthesis”, *International Conference on Application-specific Systems, Architectures and Processors*, September 2004: Acceptance Rate: 30/56 = 53.6% ([pdf](#), [slides](#))

[C26] Gang Wang, Wenrui Gong and Ryan Kastner, “System Level Partitioning for Programmable Platforms Using the Ant Colony Optimization”, *International Workshop on Logic and Synthesis (IWLS)*, June 2004 ([pdf](#)) – poster presentation

[C25] Anup Hosangadi, Farzan Fallah and Ryan Kastner, “Optimizing Polynomial Expressions by Factoring and Eliminating Common Subexpressions”, *International Workshop on Logic and Synthesis (IWLS)*, June 2004 ([pdf](#))

[C24] Wenrui Gong, Gang Wang and Ryan Kastner, “A High Performance Intermediate Representation for Reconfigurable Systems”, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, June 2004 ([pdf](#), [slides](#))

[C23] Gang Wang, Wenrui Gong and Ryan Kastner, “A New Approach for Task Level Computational Resource Bi-partitioning”, *IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS)*, November 2003 ([pdf](#), [slides](#)) – Best Paper Award Nomination

[C22] Adam Kaplan, Philip Brisk and Ryan Kastner, “Data Communication Estimation and Reduction for Reconfigurable Systems“, *Design Automation Conference (DAC)*, June 2003 – Acceptance Rate: 152/628 = 24.2% ([pdf](#), [slides](#))

[C21] Adam Kaplan, Majid Sarrafzadeh and Ryan Kastner, “High-Level Data Communication Optimization for Reconfigurable Systems“, *Workshop on Software Support for Reconfigurable Systems (SSRS)*, co-located with the *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2003 ([pdf](#))

[C20] Philip Brisk, Adam Kaplan, Ryan Kastner and Majid Sarrafzadeh, “Instruction Generation and Regularity Extraction for Reconfigurable Processors“, *International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, October 2002 ([pdf](#), [slides](#))

[C19] Ryan Kastner, Christina Hsieh, Miodrag Potkonjak and Majid Sarrafzadeh, “On the Sensitivity of Incremental Algorithms for Combinatorial Auctions“, *International Workshop on Advanced Issues of E-Commerce and Web-Based Information Systems (WECWIS)*, June 2002 ([pdf](#), [slides](#))

[C18] Elaheh Bozorgzadeh, Seda Ogrenci Memik, Ryan Kastner and Majid Sarrafzadeh, “Pattern Selection: Customized Block Allocation for Domain-Specific Programmable Systems“, *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, June 2002 ([pdf](#))

[C17] Elaheh Bozorgzadeh, Seda Ogrenci Memik, Ryan Kastner, and Majid Sarrafzadeh, “Pattern Selection in Programmable Systems”, *International Symposium of Field Programmable Gate Arrays (FPGA)*, February 2002 ([pdf](#)) – poster presentation

[C16] Ryan Kastner, Seda Ogrenci Memik, Elaheh Bozorgzadeh and Majid Sarrafzadeh, “Instruction Generation for Hybrid Reconfigurable Systems“, *International Conference on Computer-Aided Design (ICCAD)*, November 2001 – Acceptance Rate: 30.56% ([pdf](#), [slides](#))

[C15] Seda Ogrenci Memik, Elaheh Bozorgzadeh, Ryan Kastner and Majid Sarrafzadeh, “A Super-Scheduler for Embedded Reconfigurable Systems“, *International Conference on Computer-Aided Design (ICCAD)*, November 2001 – Acceptance Rate: 30.56% ([pdf](#))

[C14] Xiaojian Yang, Ryan Kastner and Majid Sarrafzadeh, “Congestion Reduction During Placement Based on Integer Programming“, *International Conference on Computer-Aided Design (ICCAD)*, November 2001 – Acceptance Rate: 30.56% ([pdf](#), [slides](#))

[C13] Andrew B. Kahng, Ryan Kastner, Stefanus Mantik, Majid Sarrafzadeh and Xiaojian Yang, “Studies of Timing Structural Properties for Early Evaluation of Circuit Design“, *Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI)*, October 2001 ([pdf](#), [slides](#))

[C12] Elaheh Bozorgzadeh, Ryan Kastner and Majid Sarrafzadeh, “Creating and Exploiting Flexibility in Steiner Trees“, *Design Automation Conference (DAC)*, June 2001 – Acceptance Rate: 160/410 = 39% ([pdf](#), [slides](#))

[C11] Ryan Kastner, Elaheh Bozorgzadeh and Majid Sarrafzadeh, “An Exact Algorithm for Coupling-Free Routing“, *International Symposium on Physical Design (ISPD)*, April 2001 ([pdf](#), [slides](#))

[C10] Xiaojian Yang, Ryan Kastner and Majid Sarrafzadeh, “Congestion Estimation during Top-down Placement“, *International Symposium on Physical Design (ISPD)*, April 2001 ([pdf](#), [slides](#))

[C9] Majid Sarrafzadeh, Elaheh Bozorgzadeh, Ryan Kastner and Ankur Srivastava, “Design and Analysis of Physical Design Algorithms“, *International Symposium on Physical Design (ISPD)*, April 2001 ([pdf](#), [slides](#))

[C8] Seda Ogrenci Memik, Elaheh Bozorgzadeh, Ryan Kastner and Majid Sarrafzadeh, “Strategically Programmable Systems“, *Reconfigurable Architecture Workshop (RAW)*, April 2001 ([pdf](#))

[C7] Ryan Kastner, Elaheh Bozorgzadeh and Majid Sarrafzadeh, “Predictable Routing“, *International Conference on Computer-Aided Design (ICCAD)*, November 2000 – Acceptance Rate: 86/265 = 32.5% ([pdf](#), [slides](#))

[C6] Ankur Srivastava, Ryan Kastner and Majid Sarrafzadeh, “Timing Driven Gate Duplication: Complexity Issues and Algorithms“, *International Conference on Computer-Aided Design (ICCAD)*, November 2000 – Acceptance Rate: 86/265 = 32.5% ([pdf](#), [slides](#))

[C5] Ryan Kastner, Elaheh Bozorgzadeh and Majid Sarrafzadeh, “Coupling Aware Routing“, *International ASIC/SOC Conference*, September 2000 ([pdf](#), [slides](#))

[C4] Ankur Srivastava, Ryan Kastner and Majid Sarrafzadeh, “Complexity Issues in Gate Duplication“, *International Workshop on Logic Synthesis (IWLS)*, June 2000 ([pdf](#))

[C3] Kiarash Bazargan, Ryan Kastner, Seda Ogrenci and Majid Sarrafzadeh, “A C to Hardware/Software Compiler“, *Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 2000 ([pdf](#)) – poster presentation

[C2] Ryan Kastner, Kiarash Bazargan and Majid Sarrafzadeh, “Physical Design for Reconfigurable Computing Systems using Firm Templates“, *Workshop on Reconfigurable Computing (WoRC)*, October 1999 ([pdf](#), [slides](#))

[C1] Kiarash Bazargan, Ryan Kastner and Majid Sarrafzadeh, “3-D Floorplanning: Simulated Annealing and Greedy Placement Methods for Reconfigurable Computing Systems“, *International Workshop on Rapid System Prototyping (RSP)*, June 1999 ([pdf](#))

Research Support (since 2007)

| Title | Granting agency | Amount of total award (include indirect costs) | Time period of contract/grant | Role (e.g. PI, co-investigator, project leader, etc.) List co-PIs/corresponding share of total award (total must = 100%) |
|--|-----------------------------|--|-------------------------------|---|
| “Architecture and Design Tools for Software Defined Acoustic Modems”, | National Science Foundation | \$180,000 | 2007-2010 | P.I. |
| CSRO: An Open Architecture, Low Power, Low Cost Underwater Modem | CalIT2 | \$46,478 | 2010-2011 | P.I. |
| Curriculum Development: Intel® Atom™ Processor in Embedded Systems courses | Intel | \$57,000 | 2010-2011 | P.I. |
| Research Experience for Undergraduates | National Science Foundation | \$16,000 | 2010-2011 | P.I. |
| “Engineers for Exploration” | National Geographic Society | \$60,000 | 2010-2011 | Co-P.I. |
| “Los Alamos - UC San Diego Educational Collaboration” | Los Alamos National Lab | \$1,764,710 | 2009-2010 | Task Leader |

Ryan Kastner – Curriculum Vitae
kastner@ucsd.edu

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|---|---|-------------|-----------|---|
| “3Dsec: Trustworthy System Security through 3-D Integrated Hardware” | National Science Foundation | \$1,500,000 | 2010-2013 | * PI on NSF award to UC San Diego 100% of \$450,000 distributed to UC San Diego - \$1.5 million was distributed to 3 institutions (UCSD, UCSB, and NPS) |
| “REU Supplement: 3Dsec: Trustworthy System Security through 3-D Integrated Hardware” | National Science Foundation | \$16,000 | 2012-2013 | P.I. |
| “Simulate & Eliminate - A Design Tool for Application Specific Processor Architectures” | Intel | \$100,000 | 2010-2011 | P.I. |
| “Automated Techniques for Detection and Identification of Fishes” | National Oceanographic and Atmospheric Administration | \$30,000 | 2010-2011 | P.I. |
| “Biplanar Interferometric Imaging Hardware Acceleration System” | National Oceanographic and Atmospheric Administration | \$24,000 | 2010-2011 | P.I. |
| “Networked Sensor Swarm of Underwater Drifters” | National Science Foundation | \$1,199,986 | 2010-2013 | Co-P.I. |
| “REU Supplement: Networked Sensor Swarm of Underwater Drifters” | National Science Foundation | \$16,000 | 2011-2012 | P.I. |
| “REU Supplement: Networked Sensor Swarm of Underwater Drifters” | National Science Foundation | \$16,000 | 2012-2013 | P.I. |
| “Engineers for Exploration” | National Geographic Society | \$60,000 | 2011-2012 | Co-P.I. |
| “Electron Tomography in the National Center for Microscopy and Imaging Research” | UCSD Chancellor’s Interdisciplinary Collaboratories Program | \$67,500 | 2011-2012 | Co-P.I. |
| “Furthering the Atom based Embedded System Education | Intel | \$30,000 | 2011-2012 | P.I. |

| Curriculum” | | | | |
|---|---|-------------|-----------|---|
| “Hardware System for Real-Time, Biplanar-Interferometric, Georeferenced Solutions from Simrad EK60 and ME70 Echosounder Data” | National Oceanographic and Atmospheric Administration | \$50,000 | 2011-2012 | P.I. |
| “EAGER: Computer Architectures and Algorithms for Adaptive Human Computer Interfaces” | National Science Foundation | \$150,000 | 2011-2012 | Co-P.I. |
| “Equipment Donation: PSoC Boards” | Cypress Semiconductor | \$10,200 | 2011 | P.I. |
| “FPGA Curriculum Development” | Xilinx | \$50,000 | 2012 | P.I. |
| “Software Donation” | Xilinx | \$211,000 | 2012 | P.I. |
| “Machine Vision and Image Processing” | Cognex | \$100,000 | 2012 | P.I. |
| “Android Phones: Equipment Donation” | Google | \$2,400 | 2012 | P.I. |
| “FPGA AutoESL Software” | Xilinx | \$119,750 | 2012 | P.I. |
| “FPGA ZED Development Boards” | Xilinx | \$16,700 | 2012 | P.I. |
| “Levenberg-Marquardt Hardware Development” | Lumedyne | \$18,000 | 2012 | P.I. |
| “OpenCV Acceleration” | Renesas Electronics Corp | \$14,500 | 2012 | P.I. |
| “Thunderbolt” | KETI/TLi | \$200,000 | 2012-2013 | P.I. |
| “Differential Power Analysis Test Equipment” | National Instruments | \$50,000 | 2012 | P.I. |
| “STTR: Scenario Based Radio Simulator and Analysis Tool” | Toyon | \$305,000 | 2012-2014 | P.I. |
| “Building Critical Systems with Verifiable | National Science Foundation | \$1,200,000 | 2012-2015 | * PI on NSF award to UC San Diego 100% of \$400,000 |

Ryan Kastner – Curriculum Vitae
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|--|-----------------------------|-----------|-----------|--|---|
| Properties Using Gate Level Analysis” | | | | | distributed to UC San Diego - \$1.2 million was distributed to 2 institutions (UCSD and UCSB) |
| “REU Supplement: Building Critical Systems with Verifiable Properties Using Gate Level Analysis” | National Science Foundation | \$16,000 | 2012-2013 | | P.I. |
| “Designing Apps on Android Classes” | Google | \$6,800 | 2012 | | P.I. |
| “Engineers for Exploration” | Intel | \$50,000 | 2012 | | P.I. |
| “CSRO: Multi-Sensor Fusion for Locating, Monitoring Foraging and Breeding Behavior, and Assessing Habitat Use of Whale Sharks” | Calit2 | \$55,000 | 2012-2013 | | P.I. |
| “REU Site: Engineers for Exploration” | National Science Foundation | \$380,000 | 2013-2016 | | P.I. |
| DragonBoard Equipment Donation | Qualcomm | \$19,920 | 2013 | | P.I. |
| “Hardware Acceleration of DNA Sequencing” | BioNano Genomics | \$23,000 | 2013 | | P.I. |
| “I-Corps: Provable Hardware Design for Integrity and Security” | National Science Foundation | \$50,000 | 2013 | | P.I. |
| “Vivado Software” | Xilinx | \$171,249 | 2013 | | P.I. |
| “FPGA Development Boards” | Altera | \$32,985 | 2013 | | P.I. |
| “RIFFA for Altera FPGAs” | Altera | \$32,000 | 2013 | | P.I. |
| “Hardware Acceleration for Machine Vision” | Cognex | \$125,000 | 2013 | | P.I. |
| “INSPIRE: Distributed Sensing Collective to Capture 3D Soundscapes” | National Science Foundation | \$993,748 | 2013-2017 | | Co-P.I. |
| “Galileo Development | Intel | \$2800 | 2014 | | P.I. |

| Boards” | | | | |
|--|--|-----------|-----------|----------------|
| “RIFFA for Xilinx FPGAs” | Xilinx | \$60,000 | 2014 | P.I. |
| “Compressed Sensing Architectures” | Cognex | \$125,000 | 2014 | P.I. |
| “Contextual Robotics” | Qualcomm | \$50,000 | 2014 | P.I. |
| “Drone Surveys for Endangered Birds” | USDA | \$188,000 | 2014 | Co-P.I. |
| “Hardware Accelerated Cell Sorting” | Cytovale | \$40,000 | 2014 | P.I. |
| “Embedded Systems Curriculum Development” | Intel | \$25,000 | 2014 | P.I. |
| “Hardware Security using 3D Integrated Circuits” | US Navy | \$150,000 | 2014-2015 | P.I. |
| “Mapping and Visualizing Complex, Large Scale Underwater Archaeological Sites and Artifacts” | California Institute for Telecommunications and Information Technology | \$40,000 | 2014-2015 | P.I. |
| “Aerial Sensing for the Maya Jungle” | California Institute for Telecommunications and Information Technology | \$50,000 | 2014-2015 | Co-P.I. |
| “Frontiers of Innovations Scholar Program” | UCSD | \$62,000 | 2015 | P.I. |
| “TWC: Small: Employing Information Theoretic Metrics to Quantify and Enhance the Security of Hardware Designs” | National Science Foundation | \$516,000 | 2015-2018 | P.I. |
| “CPS: Synergy: Towards Foundational Verification of Cyber-Physical Systems” | National Science Foundation | \$700,000 | 2015-2018 | Co-P.I. |